

CLAIMS

What is claimed is:

- 1 1. An integrated circuit comprising:
 - 2 circuitry;
 - 3 a bond pad coupled to the circuitry and for interfacing the circuitry with
 - 4 an external circuit; and
 - 5 a special contact pad coupled to the circuitry, the special contact pad for
 - 6 use only when testing the circuitry.

- 1 2. The integrated circuit of claim 1, wherein the special contact pad is smaller
2 than the bond pad.

- 1 3. The integrated circuit of claim 1, wherein the special contact pad has a
2 maximum dimension of approximately 10 microns.

- 1 4. The integrated circuit of claim 1, wherein the special contact pad is
2 structured to receive a spring contact element.

- 1 5. The integrated circuit of claim 1, wherein the special contact pad is for
2 communicating test data to the circuitry.

- 1 6. The integrated circuit of claim 1, wherein the special contact pad is for
2 communicating data from the circuitry.

- 1 7. The integrated circuit of claim 1, wherein the special contact pad is for
2 contacting a circuit node internal to the circuitry.

- 1 8. An integrated circuit comprising:
 - 2 a plurality of circuits;

3 a plurality of bond pads each coupled to at least one of the plurality of
4 circuits, the plurality of bond pads for interfacing the plurality of circuits with
5 circuits external to the integrated circuit; and

6 a plurality of special contact pads each coupled to at least one of the
7 plurality of circuits and providing an electrical contact for communicating
8 with the plurality of circuits.

1 9. The integrated circuit of claim 8, wherein the bond pads are arranged in a
2 first predetermined alignment and the special contact pads are arranged in
3 a second predetermined alignment.

1 10. The integrated circuit of claim 8, wherein the bond pads are disposed along
2 the periphery of the integrated circuit, and at least one of the special
3 contact pads is not disposed on the periphery of the integrated circuit.

1 11. The integrated circuit of claim 8, wherein the bond pads are aligned in a
2 grid pattern on the integrated circuit, and at least one of the special contact
3 pads is not aligned in the grid pattern.

1 12. The integrated circuit of claim 8, wherein the bond pads are aligned in a
2 lead-on-center configuration, and at least one of the special contact pads is
3 not aligned in the lead-on-center configuration.

1 13. The integrated circuit of claim 8, wherein the special contact pads are
2 smaller than the bond pads.

1 14. The integrated circuit of claim 8, further comprising a spring contact
2 element attached to one of the special contact pads.

1 15. The integrated circuit of claim 8, wherein at least one of the special contact
2 pad is electrically disposed between two of the plurality of circuits to
3 monitor signals transmitted between circuits.

1 16. The integrated circuit of claim 8, wherein one of the special contact pads
2 communicates test data to one of the circuits, and another one of the
3 special contact pads communicates an output of the circuit.

1 17. The integrated circuit of claim 8, wherein one of the special contact pads
2 communicates test data to the one of the circuits, and one of the bond pads
3 communicates an output of the circuit.

1 18. The integrated circuit of claim 8, wherein one of the bond pads
2 communicates test data to one of the circuits, and one of the special contact
3 pads communicates an output of the circuit.

1 19. The integrated circuit of claim 8, wherein in a first mode of operation one
2 of the special contact pads communicates data to one of the circuits, and in
3 a second mode of operation the special contact pads communicates data
4 from the circuit.

1 20. The integrated circuit of claim 8, wherein one of the plurality of circuits is
2 an embedded memory array, and the special contact pads communicates
3 address and test data to the embedded memory array.

1 21. The integrated circuit of claim 8, wherein one of the plurality of circuits
2 includes programmable circuitry, and the special contact pads are for
3 communicating signals for programming the programmable circuitry.

1 22. The integrated circuit of claim 8, wherein the bond pads are structured to
2 be connected to external circuitry by bonding wires, and the special contact

3 pads are not structured to be connected to external circuitry by bonding
4 wires.

1 23. The integrated circuit of claim 8, wherein the bond pads are structured to
2 be connected to external circuitry by solder bumps, and the special contact
3 pads are not structured to be connected to external circuitry by solder
4 bumps.

1 24. The integrated circuit of claim 8, wherein the bond pads are structured to
2 be in electrical contact with a package for housing the integrated circuit,
3 and the special contact pads are not structured to be in electrical contact
4 with the package.

1 25. The integrated circuit of claim 8, wherein the plurality of circuits includes
2 a first circuit and a second circuit having a redundant function of the first
3 circuit, and wherein the special contact pads are disposed about the first
4 and second circuits to communicate with the first and second circuits.

1 26. The integrated circuit of claim 25, further comprising means for
2 communicating with the special contact pads and for disabling the first
3 circuit if it is defective and for enabling the second circuit.

1 27. The integrated circuit of claim 25, further comprising means for
2 communicating with the special contact pads and for disabling the second
3 circuit.

1 28. The integrated circuit of claim 8, further comprising electrostatic discharge
2 protection circuitry for the bond pads and not for the special contact pads.

1 29. An integrated circuit comprising:
2 a plurality of bond pads;

3 an internal circuit not directly monitorable by the bond pads; and
4 at least one special contact pad for directly accessing the internal circuit.

1 30. The integrated circuit of claim 29, wherein the internal circuit comprises
2 an embedded memory array, and the at least one special contact pad
3 communicates address and memory data with the embedded memory
4 array.

1 31. The integrated circuit of claim 29, wherein the internal circuit comprises
2 programmable circuitry, and the at least one special contact pad
3 communicates programming signals to the programmable circuitry.

1 32. The integrated circuit of claim 29, wherein the bond pads are arranged in a
2 first predetermined alignment and the at least one special contact pad is in
3 a second predetermined alignment.

1 33. The integrated circuit of claim 29, wherein the at least one special contact
2 pad is smaller than the bond pads.

1 34. The integrated circuit of claim 29, further comprising a spring contact
2 element attached to the at least one special contact pad.

1 35 A package for housing an integrated circuit, comprising:
2 a plurality of terminals for testing the overall operation of the
3 integrated circuit; and
4 a special contact pad for directly accessing an internal circuit of the
5 integrated circuit.

1 36. The package of claim 35, wherein the special contact pad is for
2 communicating test signals for the integrated circuit.

- 1 37. The package of claim 35, wherein the special contact pad is for
- 2 communicating test signals from the integrated circuit.

- 1 38. The package of claim 35, wherein the contact pads are aligned in a grid
- 2 pattern on the integrated circuit, and the special contact pads is not aligned
- 3 in the grid pattern.

- 1 39. The package of claim 35, wherein the package comprises a ball-grid-array
- 2 (BGA) package and the contact pads include contact balls.

- 1 40. The package of claim 35, wherein the special contact pad is smaller than
- 2 the contact pad.

- 1 41. The package of claim 35, wherein the special contact pad has a maximum
- 2 dimension of approximately 10 microns.

- 1 42. A method of testing circuitry in an integrated circuit having bond pads
- 2 and a special contact pad, the method comprising:
 - 3 providing test signals to the circuitry; and
 - 4 monitoring an output of the circuitry through the special contact pad.

- 1 43. A method of testing circuitry in an integrated circuit having bond pads
- 2 and a special contact pad, the method comprising:
 - 3 providing test signals to the circuitry through the special contact pad;
 - 4 and
 - 5 monitoring an output of the circuitry through the bond pad.

- 1 44. A method of testing an integrated circuit having bond pads and a special
- 2 contact pad, the method comprising:
 - 3 providing test signals to a first circuit through at least one of the bond
 - 4 pads;

5 monitoring an output of the first circuit through the special contact
6 pad;
7 providing the output of the first circuit to a second circuit; and
8 providing an output of the second circuit to at least another one of the
9 bond pads.

1 45. A method of testing an integrated circuit on a wafer, comprising:
2 electrically contacting a first test substrate to special contact pads
3 disposed on the integrated circuit; and
4 electrically contacting a second test substrate to bond pads disposed on
5 the integrated circuit.

1 46. A probe card comprising:
2 a first probe element for contacting bond pads of an integrated circuit;
3 and
4 a second probe element for contacting a special contact pad of the
5 integrated circuit

1 47. The probe card of claim 46, wherein the first and second probe elements
2 comprise cantilevered probes.

1 48. The probe card of claim 46, wherein the first and second probe elements
2 comprise contact balls.

1 49. The probe card of claim 46, further comprising a plurality of the first probe
2 elements arranged in a first predetermined alignment, and wherein the
3 second probe element is arranged in a second predetermined alignment.

1 50. The probe card of claim 49, wherein the predetermined alignment is a grid
2 pattern.

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- 1 51. The probe card of claim 49, wherein the predetermined alignment is a
- 2 rectangular pattern.
- 1 52. The probe card of claim 49, wherein the first and second probe elements
- 2 have different lengths.
- 1 53. The probe card of claim 49, wherein the first and second probe elements
- 2 are spring contact elements.
- 1 54. The probe card of claim 53, wherein the spring contact elements include
- 2 pyramid-shaped tip contact structures.
- 1 55. The probe card of claim 49, wherein the first and second probe
- 2 elements are COBRA-style probes.
- 1 56. An apparatus for communicating signals with an internal circuit node and
- 2 input/output (I/O) node of a semiconductor device, comprising:
 - 3 a first contact element for communicating signals with the internal
 - 4 circuit node; and
 - 5 a second contact element for communicating signals with the I/O node.
- 1 57. The apparatus of claim 56, wherein the first contact element comprises a
- 2 resilient contact element.
- 1 58. The ~~apparatus of~~ claim 57, wherein the second contact element comprises
- 2 a ~~resilient contact~~ element.
- 1 59. The apparatus of claim 56, wherein the first and second contact elements
- 2 have different lengths.
- 1 60. A method of communicating a signal to an internal circuit node of a
- 2 semiconductor device, comprising:

3 contacting a special contact pad that is electrically coupled to the
4 internal circuit node; and
5 transferring electrical energy through the special contact pad to the internal
6 circuit node.

1 61. A socket for releasably connecting a first electronic component to a second
2 electronic component, comprising:

3 a first plurality of resilient contact structures extending upward from a
4 top surface of a support substrate, the first plurality of resilient contact
5 structures for communicating signals with a first plurality of contact points of
6 the first electronic component;

7 a second plurality of resilient contact structures extending upward from
8 the top surface of the support substrate, the second plurality of resilient
9 contact structures for communicating signals with a second plurality of
10 contact points of the second first electronic component; and

11 a plurality of contact structures disposed on a bottom surface of the
12 support substrate, selected ones of the contact structures are connected
13 through the support substrate to selected ones of the resilient contact
14 structures.

1 62. The socket of claim 61, wherein the second electronic component is a
2 circuit board.

1 63. The socket of claim 61, further comprising means for receiving the first
2 electronic component.

1 64. The socket of claim 61, further comprising means for urging the first
2 electronic component down onto the first and second resilient contact
3 elements.